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NRL Report 8532

## **Ranging and Synchronization Between Nominally Co-Orbital Satellites**

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## RANGING AND SYNCHRONIZATION BETWEEN NOMINALLY CO-ORBITAL SATELLITES

### I. INTRODUCTION

A link between two satellites can provide direct measurements of intersatellite range and clock synchronism that are more accurate than estimates obtainable from ground measurements. Moreover, these direct measurements can be made continuously with near-zero delays. Intersatellite links for ranging and synchronization are likely to have application in distributed satellite systems acting as sparsely filled arrays of large dimension such as long-baseline interferometers. They are also likely to be applied in experiments performed from satellites orbiting in proximity to the Space Shuttle in the laboratory sortie mode, and in other multiple satellite experiments.

In this report, we are principally concerned with measuring range between two satellites with accuracy of about 1 m, and adjusting the clock on one satellite so that its phase is kept within several nanoseconds of the phase of the clock on the other satellite. At this level of accuracy, vector distances from one point to another on the same satellite are readily obtainable, and commercially available digital logic is adequate. Better accuracy will require faster logic which is now available only in custom hardware, and can involve sophisticated means to measure vector distances and delays between points on a satellite.

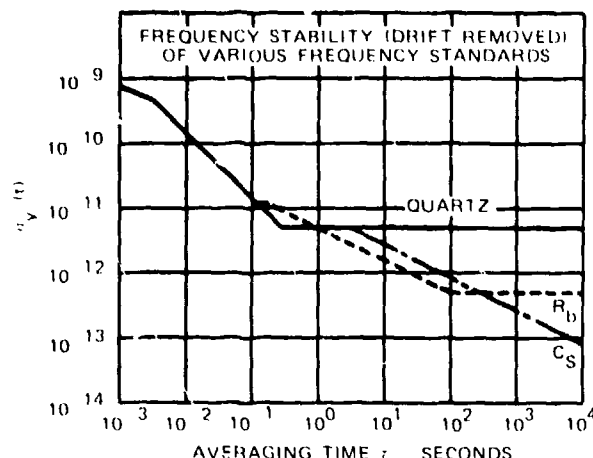
These accuracy goals can be tightened somewhat for a given application if it is acceptable to process longer and/or to measure clock asynchronism without actually adjusting either clock thus avoiding the inaccuracies in the adjustment process. Digital clocks and other digital implementations are employed because of difficulties in calibrating bias errors in analog devices. The goals for measurement accuracy can be made more stringent if the desire is to monitor changes in the phase of one satellite clock relative to that of the other, and changes in the intersatellite range instead of measuring *actual* phase differences and distances. Then, bias errors would be of less concern and analog techniques may be substituted to improve precision.

### II. TIMING SOURCES AND RANGE PROFILES

Each satellite is assumed to have a stable frequency source that generates a digital clock signal at the rate of 400 Mpps. This clock frequency is chosen because it represents the present limit for commercially available logic devices. Higher rates require custom designs which would be warranted in only special applications. The synchronization process seeks to apply phase references to the clocks on each satellite so that the two phase references are as close to each other as possible without making phase adjustments to the clock pulses themselves. Since there is a 2.5 ns interval between clock pulses, even a perfect choice for phases on the two clocks can result in a difference of as much as 1.25 ns or an RMS error of 0.72 ns. This represents a lower bound on the accuracy in synchronizing the two clocks.

Figure 1 summarizes the stability of various time standards. Data points from typical stable oscillators designed for use in spacecraft were found to lie on the quartz curve shown. The system discussed in Section III will be able to detect and correct an error in synchronization in a time

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|                           |                               |
|---------------------------|-------------------------------|
| VERY SHORT TERM (< 0.1 S) | < .01 NS                      |
| SHORT TERM (1 S - 1 H)    | $\sim 10^{-11}_t$             |
| LONG TERM DRIFT           | $< 5 \times 10^{-10}$ PER DAY |
|                           | $(< 10^{-6}$ AFTER 6 YEARS)   |
| SETTABILITY               | $\sim 5 \times 10^{-8}$       |

Fig. 1 — Stability of typical frequency standards. Plot is taken from Ref. 1. Data points taken from several satellite oscillators agree with the quartz curve shown. Estimates for stability to 1 h are taken from the plot; estimates for long term drift and settability were obtained separately.

interval somewhat greater than the two-way path delay between satellites. In most applications envisioned, this time interval will be less than a few milliseconds. Figure 1 indicates that clock variance in that time will be about 0.01 ns. At the beginning of life, the frequency offset is governed by the settability which leads to errors of only 0.01 ns after 1 ms. At the end of life, frequency offset can lead to errors of almost 1 ns after 1 ms, but this error source is slowly varying and can be compensated without real-time measurements. Clearly system accuracy is going to be governed by measurement accuracy and not by loop delays and clock stability.

Figure 2 tabulates the maximum range rates estimated for the major perturbative sources. The largest contribution will be from any range variations due to intentional differences in satellite orbits. These will be periodic with periods equal to one-half the orbital period. However, this motion is deterministic and, if necessary, can be corrected routinely without real-time measurements. (Its major impact on ranging and synchronization is as a source of doppler which affects tracking loop bandwidths and frequency offsets.)

The contributions of other natural phenomena and orbital adjustments are estimated (by educated guesswork) to give rise to maximum range rates on the order of 1 m/s. Depending on the complexity of the prediction model used, it is estimated that the indeterminate motion due to all sources can be reduced to the order of 1 m/min. To maintain a range accuracy of 1 m, corrections must be made at a rate somewhat greater than once per second. Corrections can be based on predictions or by direct measurement. However, from the above estimates, even with complex prediction models, direct measurements will be needed on the order of once per minute. The required rates for ranging and synchronization appear to be about the same. Conveniently, the same measurements serve both purposes.

| <u>SOURCE</u>               | <u>MAXIMUM<br/>RANGE RATE</u> | <u>INDETERMINANT<br/>RESIDUE</u> |
|-----------------------------|-------------------------------|----------------------------------|
| PERIODIC MOTION             | -                             | O [1 M/MIN]                      |
| DIFFERENCE IN ORBIT HEIGHTS | O [1 M/S]                     |                                  |
| GEOID                       |                               |                                  |
| DRAG DIFFERENTIAL           |                               |                                  |
| THRUSTING                   |                               |                                  |

Fig. 2 — Range instabilities

### III. RANGING AND SYNCHRONIZATION (R&S) SYSTEM

In many applications, we foresee a need to transfer high-rate digital data between satellites. Therefore we have given attention to implementations in which the data stream is also used for time transfer. Some of our design preferences are based on this assumption, and so it is convenient to discuss the R&S system on this basis. Section IV will consider alternative waveform systems.

R&S system options can be put into two classes referred to here as "full-loop" and "balanced" systems. In a full-loop system, ranging is performed on only one satellite at a time; in the balanced system both satellites are making time-difference measurements simultaneously. The same accuracy seems to be achievable with either system, but for this application a balanced system provides advantages in implementation. The balanced system option will be presented, its performance discussed, and then contrasted with a full-loop system.

#### A. System Description

Figure 3 illustrates a balanced system for purposes of this discussion. The digital signal transmitted from each satellite is locked to its clock, and on each satellite the time difference between its clock and the clock derived from the signal received from the other satellite is measured. The satellites transmit the measured time differences to each other, and these differences are compared. The two clocks are in synchronism if, after adjustment for differences in equipment delays on the forward and backward links, the two measurements are equal. If they are not equal, the system provides the proper correction to bring the slave clock into synchronism with the master (indicated by the dashed line in Fig. 3).

Figure 4 illustrates the crosslink data format. Information is transmitted at a fixed rate in a series of fixed-length frames which begin with a frame-synch word (FSW) and include a time-difference word and frame identification as well as data words. The FSWs are benchmarks for the satellite clock. The start of the FSW of the  $i$ th frame on the master satellite is generated at time  $T_{iM}$ ; on the slave it is generated at  $T_{iS}$ . If  $T_{iS} = T_{iM}$ , the two clocks are synchronized at that instant. The time on the slave at which the start of the  $i$ th FSW arrives from the master is designated as  $(T_{iM})_S$ ; similarly the start of the  $i$ th FSW from the slave is said to arrive at the master at time  $(T_{iS})_M$ . The time difference

$$\tau_{iS} = (T_{iM})_S - T_{iS} \quad (3.1)$$

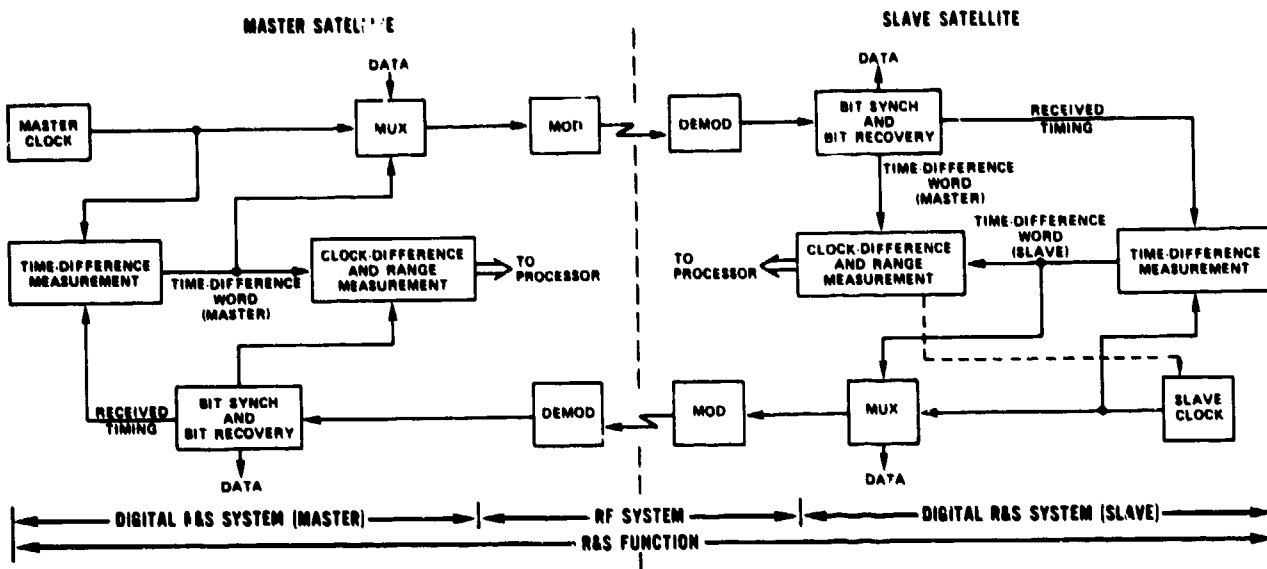


Fig. 3 - Balanced system block diagram and task breakdown

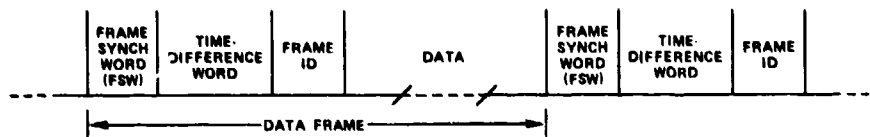


Fig. 4 - Data frame format

is measured on the slave, and

$$\tau_{iM} = (T_{iS})_M - T_{iM} \quad (3.2)$$

is computed on the master. The received times are given by

$$(T_{iM})_S = T_{iM} + d_f + R \quad (3.3)$$

$$(T_{iS})_M = T_{iS} + d_r + R \quad (3.4)$$

where  $R$  is time delay in the free space path between satellites,

$d_f$  is equipment delay in the path from master to slave, and

$d_r$  is equipment delay in the path from slave to master.

It follows that the time difference measurements can be written as

$$\tau_{iS} = (T_{iM} - T_{iS}) + d_f + R \quad (3.5)$$

and

$$\tau_{iM} = (T_{iS} - T_{iM}) + d_r + R. \quad (3.6)$$

Finally, by alternately subtracting and adding Eqs. (3.5) and (3.6) we obtain the expressions

$$(T_{iS} - T_{iM}) = \frac{(\tau_{iM} - \tau_{iS}) + (d_f - d_r)}{2} \quad (3.7)$$

and

$$R = \frac{(\tau_{iM} + \tau_{iS}) - (d_f + d_r)}{2}. \quad (3.8)$$

The essential information for synchronization and ranging is given by Eqs. (3.7) and (3.8), respectively. Equation (3.7) gives the time difference, if any, between the two clocks at time  $T_i$ ; Eq. (3.8), when divided by the velocity of propagation (0.3 m per ns), yields the range between satellites. If an error in clock synchronization is present at  $T_i$ , the correction cannot be applied in less than the round trip delay time which is equal to  $2R$  plus equipment and computational delays. If the maximum range between satellites is 100 nmi,  $2R < 1.2$  ms. Therefore time corrections can typically be applied within a millisecond.

## B. Frequency Source on Slave

Figure 3 shows the slave clock being derived from a free-running oscillator on the slave. By adding or subtracting pulses, the R&S system defines the epoch by associating particular time pulses with the start of frame. Aside from these rather rare additions and subtractions, the clock rate is set by the free-running oscillator in the slave.

An alternative is to use the incoming signal from the master to provide the basic frequency on the slave. The signal, which would come off the bit synchronizer, would differ in frequency from the master clock by only the doppler shift due to satellite motion. This is typically very small—much smaller than the worst-case clock drift.

Each of these implementations has advantages. The free-running oscillator (Fig. 3) makes performance less sensitive to jitter in the bit synchronizer and to noise, interference, and doppler in the crosslink. It also allows (degraded) system operation in the event of crosslink failure. The alternative implementation makes performance insensitive to long-term drifts and provides a means to operate in the event of R&S system failures (see discussion of full-loop systems). For these reasons, it seems advantageous to provide both implementations, selectable by ground command.

## C. Actual vs Computed Synchronization

In theory, the same performance can be achieved either by bringing the clocks into synchronization as indicated in Fig. 3 or by making the time-difference measurements, computing the amount



of asynchronism, and then compensating for it in the processing. In practice, it probably simplifies the overall system to actually synchronize the clocks, but because of the quantization inherent in a digital system the accuracy with which the synchronization can be achieved is going to be limited by the clock period.

#### D. Full-loop System

As mentioned, R&S system options can be characterized as "balanced" or "full-loop." In the full-loop system, time-difference measurements are made on only one satellite. Figure 5 shows a full-loop system in which the slave clock is locked to the incoming signal from the master, and the signal from the slave is locked to the slave clock. If the  $i$ th FSW is received and retransmitted on the slave at  $T_{iS}$ , it must have been transmitted from the master at  $T_{iS} - (R + d_f)$ , and after retransmission it will be received back at the master at  $T_{iS} + (R + d_r)$ . For synchronization to exist  $T_{iM} = T_{iS}$  so that the master wants to set the time advance (using the dashline in Fig. 5) to be  $\Delta = (R + d_r)$ .<sup>\*</sup> This can be accomplished by making  $\Delta$  equal to the time measurement  $\tau_{iM} = (T_{iS})_M - T_{iM}$  (with correction for any difference between  $d_f$  and  $d_r$ ):

$$\Delta - d_r = \tau_{iM} - d_f. \quad (3.9)$$

The minimum interval from  $T_i$  to the time when a correction to the slave clock can be made is  $3R$  plus equipment and computational delays. This is about 50% longer than the corresponding interval for the balanced system. For this application the delay is not a critical limit on performance

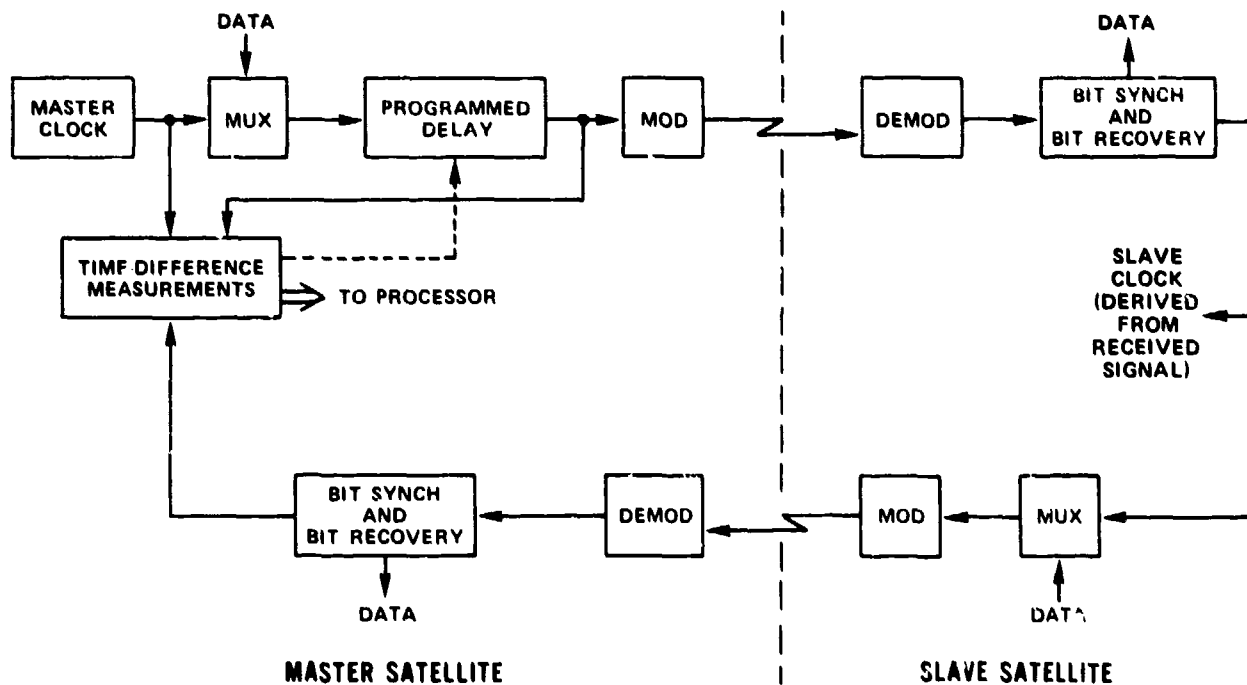


Fig. 5 — Full-loop system with programmed delay in master satellite

<sup>\*</sup>The advance  $\Delta$  can be implemented with a variable delay  $D_v = F - \Delta$  where  $F$  is the frame length. The frame on the slave is then numbered one less than the Frame ID in the received signal.

and the advantage is not significant. Further, by performing the ranging measurement on the slave, the full-loop system can yield the same delay as does the balanced system.

The principal disadvantage of the full-loop system illustrated in Fig. 5 is the need to provide storage for data in order to have the synchronized format illustrated in Fig. 4. The full-loop scheme in which ranging is performed on the slave requires a timing signal from the slave which is not synchronized to the slave clock.

Other features of the balanced system are preferred for a system which actually synchronizes the slave clocks to the master. (For example, the balanced system seems to provide a convenient means for calibration which is presented in Section V.) If instead the clocks were to run asynchronously with corrections applied in processing, the relative merits of the balanced and full-loop systems would bear reevaluation. In particular, if there is no data transfer on the crosslinks, full-loop tone or pseudonoise ranging systems with a coherent transponder on the slave satellite would be prime options.

If in the balanced system the slave clock were derived from the bit synchronizer (the alternative implementation discussed previously) and the time-difference system on the slave were disabled, a full-loop system capable of measuring but not compensating for clock asynchronism would result. Compensation performed in the processing would then permit operation in the event of some R&S system failures.

#### IV. GENERIC WAVEFORM SYSTEMS

For purposes of this discussion it is convenient to consider the RF system together with the bit synchronizer. This can be referred to as the "waveform" system.

Time transfer and ranging systems can employ waveforms which are digital, analog (tone signals), or a combination of the two. In the system described in Section III, the digital signal provides the means for time transfer and ranging. The bit synchronizer is assumed to establish the bit transition with an RMS accuracy of 1.25 ns (Section V). The data format resolves ambiguities by means of the FSW and Frame ID.

A pure analog (or tone) system employs a number of sine waves which provide the necessary accuracy and ambiguity resolution. The highest frequency tone provides the accuracy—typically  $0.001 < \sigma/T < 0.05$  where  $T$  is the tone period. Thus to provide an accuracy  $2\sigma = 2.5$  ns, the highest frequency tone would have to be between 0.8 and 40 MHz. Successively lower frequency tones, in steps of multiples of about 10 or 15, are required until the period of the lowest frequency exceeds the initial ambiguity in range and timing.

With the digital signal, time accuracy is derived by estimating the phase of bit transitions. Although ultimate limits might be the same as for resolving zero crossings of a tone, practical performance with digital signals will be further limited by any deviation of the modulator from ideal. As an example of typical performance in bit synchronization in a digital link with a bit error rate requirement of  $10^{-6}$ , the bit synchronizer will typically be designed for  $\sigma/T < 0.04$  (or poorer) where  $T$  is the bit period.

The crosslink system design began from the estimate that a bit period of about 80 ns (corresponding to 12.5 Mbps) is about what will be needed for  $2\sigma = 2.5$  ns ( $\sigma/T = 0.015$ ). To provide some safety, a Manchester coded waveform was chosen to provide transitions at a rate of 25 million per second, or a minimum period between transitions of 40 ns.

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Therefore with the rate of 12.5 Mbps, the data signal itself appears adequate for time and range transfer. If shown to be desirable after further study, the waveform could be changed to provide a higher rate digital component, or a tone can be added to provide additional resolution.

If the data rate were to be lower, a tradeoff might be required between an all-digital waveform system and a hybrid employing a tone in addition to the data signal. A pure tone system might be employed if there were no requirement for data transfer, but the problem of keeping uncalibratable biases sufficiently small might preclude a pure analog implementation.

### A. Parameters Affecting System Accuracy

The bound on jitter performance of a bit synchronizer will be of the form

$$\frac{\sigma}{T} > \frac{k}{\sqrt{nE/N_o}}, \quad (4.1)$$

where  $\sigma$  is the RMS jitter,

$T$  is symbol duration,

$k$  is a constant (typically  $0.3 < k < 0.5$ ),

$n$  is the number of transitions in an estimate,

$E$  is the signal energy per transmitted symbol,

$N_o$  is the noise spectral density, and

$E/N_o$  is the digital signal-to-noise ratio.

The signal bandwidth  $B$  is proportional to  $1/T$  so that Eq. (4.1) can be rewritten as

$$\sigma > \frac{k'}{B\sqrt{nE/N_o}}. \quad (4.2)$$

These equations indicate the dependence of the random error in time measurements on the basic parameters of bandwidth and signal-to-noise ( $E/N_o$ ). They indicate that within limits (defined by the bit synchronizer and system stabilities) it is possible to tradeoff among  $B$ ,  $E/N_o$ , and  $n$ . The performance being sought for the crosslinks with Manchester coding is

$$\sigma/T < 0.03$$

with  $T = 40$  ns and  $2\sigma < 2.5$  ns.

The bounds given by Eqs. (4.1) and (4.2) do not consider bias errors which arise from non-calibratable equipment delays and asymmetries. The noncalibratable delay and asymmetries of a given spacecraft component will arise primarily from variations in temperature and voltage and effects of aging. The exact relationship will depend on the component, but in general they will be some fraction of the total delay through that component. In turn, total delay is inversely proportional to the bandwidth of the component. Therefore, bias errors are inversely proportional to component bandwidths.

Thus the ability to trade-off among bandwidth, signal-to-noise, and integration time as would be inferred from Eqs. (4.1) and (4.2) is restricted by the fundamental role of bandwidth in bias error terms. For this reason, component bandwidths will have to be considerably greater than the signal bandwidth of about 25 MHz. Component bandwidths need not be limited to the signal bandwidth, but in some cases the potential advantage of reducing signal bandwidth is lost if the bandwidth of certain components is not similarly reduced. For example, a critical source of bias error is that of the RF filter in the receiver. Less than 1-to-1 reduction in required signal power will accrue from reducing signal bandwidth without reducing the RF filter bandwidth.

## B. Bit Synchronizer

Alternative digital and analog designs have been considered for bit synchronization. One attraction of digital implementations is an expected ease of dealing with drifts and calibrations within the bit synchronizer itself. Whether this advantage is real can only be determined after a working model exists. An analog design might have less jitter.

The baseline digital model uses a design called DTTL (data transition tracking loop) [2]. Among the advantages of the DTTL algorithm is a relative insensitivity to bias level and an ability to operate at low values of  $E/N_0$ . The advantage of insensitivity to bias level is obvious for a system that is to operate unattended for a long period of time. A special advantage of being able to operate at low  $E/N_0$  is that, if the crosslink data rate turns out to be less than 12.5 Mbps, the bit synchronizer could operate with the present waveform and repetitive bit transmission or error correcting codes.

## V. ERROR BUDGET AND SYSTEM PERFORMANCE

The limits of R&S accuracy are clearly going to be set by equipment variations and measurement inaccuracies rather than by instabilities in the system clock, satellite relative motions, and path delays. To this point error budgets and estimates on performance have been based principally on what is thought to be reasonable hardware performance. There have been some simulations and analyses and limited hardware measurements.

The R&S error budgets shown in Figs. 6 and 7 require some explanation. These entries represent hardware design goals. Each budget lists bias errors and random errors separately. First, an allocation for each bias and random error source is listed, using "worst case" numbers for quantization errors and  $2\sigma$  values for bias and noise terms. Then random and bias errors are totaled separately. The errors are algebraically summed (a worst case). The total "allocation" is obtained as follows.

a. *Synchronization Errors* — Since each error component is divided by 2 to obtain clock settings (Eq. 3.7), the allocation to timing error is obtained by dividing the allocation to differential delay by 2.

b. *Range Errors* — The contribution of each error component is divided by 2 (see Eq. 3.8) and converted from nanoseconds to meters (0.3 m per ns). Therefore, the allocation to one-way range error is obtained by multiplying the allocation to roundtrip delay error by 0.15.

The use of algebraic summing is conservative since it assumes that errors are correlated. Further, the contribution of random and quantization errors can be reduced by averaging over longer periods. Therefore, the resulting combined errors of  $\pm 5.75$  ns and  $\pm 2.64$  m are conservative upper

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|  | ALLOCATION TO<br>DIFFERENTIAL DELAY<br>ERROR (NS) | ALLOCATION TO<br>TIMING ERROR<br>(NS) |
|--|---|---------------------------------------|
| <b>BIAS ERRORS</b>                           |   |                                       |
| QUANTIZATION OF CALIBRATED DELAY<br>(MASTER) | ±1.25 (MAX)                                       |                                       |
| QUANTIZATION OF CALIBRATED DELAY<br>(SLAVE)  | ±1.25 (MAX)                                       |                                       |
| MASTER MODULATOR                             | .5 (2σ)   |                                       |
| MASTER DEMODULATOR                           | 1.5 (2σ)  |                                       |
| SLAVE MODULATOR                              | .5 (2σ)   |                                       |
| SLAVE DEMODULATOR                            | 1.5 (2σ)  |                                       |
|  | ±6.5  | ±3.25                                 |
| <b>RANDOM ERRORS</b>                         |   |                                       |
| CLOSED LOOP FILTERING OF FORWARD<br>PATH     | 1.25 (2σ)   |                                       |
| QUANTIZATION (SLAVE BIT SYNCH)               | ±1.25 (MAX)                                       |                                       |
| CLOSED LOOP FILTERING OF<br>BACKWARD PATH    | 1.25 (2σ)   |                                       |
| QUANTIZATION (MASTER BIT SYNCH)              | ±1.25 (MAX)                                       |                                       |
|  | ±5.0  | ±2.5                                  |
| TOTAL SYNCHRONIZATION ERROR (NO SMOOTHING)   |   | ±5.75 NS                              |

Fig. 6 — Budget for synchronization error sources

|   | ALLOCATION TO<br>ROUND-TRIP DELAY<br>ERROR (NS) | ALLOCATION TO<br>ONE-WAY RANGE<br>ERROR (M) |
|---|---|---|
| <b>BIAS ERRORS</b>                        |   |   |
| HARDWARE VARIATION FROM CALIBRATION       | 10 (2σ)   | ±1.5  |
| QUANTIZATION OF CALIBRATED DELAY          | ± 2.5 (MAX)                                     | ± .38                                       |
| <b>RANDOM ERRORS</b>                      |   |   |
| CLOSED LOOP FILTERING OF FORWARD<br>PATH  | 1.25 (2σ)                                       | ± .19                                       |
| QUANTIZATION (SLAVE BIT SYNCH)            | ± 1.25 (MAX)                                    | ± .19                                       |
| CLOSED LOOP FILTERING OF<br>BACKWARD PATH | 1.25 (2σ)                                       | ± .19                                       |
| QUANTIZATION (MASTER BIT SYNCH)           | ± 1.25 (MAX)                                    | ± .19                                       |
| TOTAL RANGE ERROR (NO SMOOTHING)          |   | ±2.64                                       |

Fig. 7 — Budget for range error sources

bounds with the assumed hardware performance. It should be noted that the bias terms for range are larger than for synchronization because the former involve delays while the latter involve differential delays.

#### A. Long-Term Averaging of R&S Data

To date, the design and analysis of the R&S system has focused on near-real-time clock synchronization and range estimates, with range estimates being applied directly to the estimate of in-track difference. Since random errors (largely quantization errors) are a major fraction of total error allocations, improvement can accrue through long-term averaging. Whether this should be accomplished as part of the R&S system, or be applied later in processing, needs to be determined.

The contribution which the crosslink R&S system can make to ephemeris accuracy also bears further study. Since a major component of any range rate between stationary (lead/trail) satellites is difference in altitude, estimates of the radial component of ephemeris might be improved by using range rate data. The relative cross-track motion of a dynamic satellite might provide a means for more accurate relative cross-track estimates. Further, since long-term averaging can make use of range rate as well as range, and because "biases" are sometimes not truly constant but slowly varying, the bias errors due to equipment calibration errors might be reduced. Then these improved long-term estimates might be used to provide improved calibration for direct measurements.

#### B. On-Board Calibration

Options available for meeting error budgets include:

- a. Keeping component variations within specified bounds over the spacecraft life and over full excursions in temperature and voltage.
- b. Controlling or measuring temperatures and voltages of critical components.
- c. Employing periodic on-board calibration or compensation.

Optimizing the design will require an understanding of available options. In particular, approaches to on-board calibration and compensation will be explored.

An example of a compensation (or calibration) network is shown in Fig. 8, which is a simplification of Fig. 3 with "mixers" added in each satellite as shown. The purpose of the mixers is to provide compensation loops. (The discussion assumes a "compensation" network in which equipment delays are automatically removed. The same basic design could be employed for "calibrating" delays and removing them later in processing.)

If an FSW is generated by the master clock at  $T_{OM}$  and by the slave clock at  $T_{OS}$ , the "time-difference-measuring (TDM)" box on the master will receive FSWs at three times:

$$M_1 = T_{OM}$$

$$M_2 = T_{OM} + D_{MM} + D_{MD} + D_{Mmixer}$$

$$M_3 = T_{OS} + D_{SM} + D_{MD} + D_R$$

# SCHWARTZ

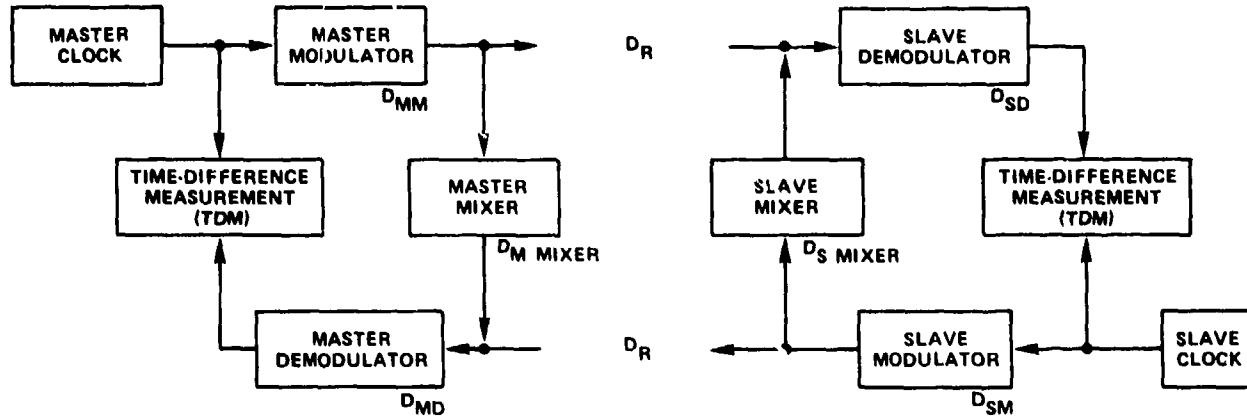


Fig. 8 — Calibration network

The TDM box on the slave will receive FSWs at times:

$$S_1 = T_{OS}$$

$$S_2 = T_{OS} + D_{SM} + D_{SD} + D_{S\text{mixer}}$$

$$S_3 = T_{OM} + D_{MM} + D_{SD} + D_R .$$

If counters in the respective boxes are started at  $M_1$  and  $S_1$  and stopped at  $M_3$  and  $S_3$ , the resulting counts would be

$$C_M = M_3 - M_1 = (T_{OS} - T_{OM}) + D_{SM} + D_{MD} + D_R$$

$$C_S = S_3 - S_1 = (T_{OM} - T_{OS}) + D_{MM} + D_{SD} + D_R .$$

Using these counts, time asynchronism and range are given by:

$$2(T_{OS} - T_{OM}) = (C_M - C_S) + (D_{MM} - D_{SM}) + (D_{SD} - D_{MD}) \quad (5.1)$$

$$2D_R = (C_M + C_S) - (D_{MM} + D_{SM}) - (D_{SD} + D_{MD}) . \quad (5.2)$$

These equations are equivalent to Eqs. (3.7) and (3.8).

If the counters are started at times  $M_2$  and  $S_2$  (instead of  $M_1$  and  $S_1$ ) and stopped at  $M_3$  and  $S_3$ , the resulting counts would be

$$C'_M = M_3 - M_2 = (T_{OS} - T_{OM}) + (D_{SM} - D_{MM}) + D_R - D_{M\text{mixer}}$$

$$C'_S = S_3 - S_2 = (T_{OM} - T_{OS}) + (D_{MM} - D_{SM}) + D_R - D_{S\text{mixer}} .$$

Using these counts, we obtain time asynchronism and range by:

$$2(T_{OS} - T_{OM}) = (C'_M - C'_S) + 2(D_{MM} - D_{SM}) + (D_{S\text{mixer}} - D_{M\text{mixer}}) \quad (5.3)$$

$$2D_R = (C'_M + C'_S) + (D_{M\text{mixer}} + D_{S\text{mixer}}). \quad (5.4)$$

Equation (5.4) clearly provides a better estimate for range than does Eq. (5.2). The only sources of bias error are the two mixers. Equation (5.3) can be expected to provide a better estimate for time asynchronism than does Eq. (5.1) because the demodulator delays are not present.

The compensation network provides an alternative to controlling the uncalibrated demodulator delays which are a critical problem in RF system design. Better understanding of the network as well as component error sources is required to evaluate design options.

## VI. ACKNOWLEDGMENTS

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## VII. REFERENCES

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